REMARKS/ARGUMENTS

Favorable reconsideration of this application as currently amended and in view of the following remarks is respectfully requested.

Claims 1-4 are currently pending. Claims 1-4 have been amended by the current amendment.

The specification has been amended to clarify that the double gate FET disclosed therein is an *insulated* double gate FET. Support for the change can be found in Figure 1 and paragraph [0008] of the specification which collectively show that the claimed methods are applied to a double gate FET having insulating layers 2 and 7. No new matter has been added.

In the outstanding office action, Figure 1 was objected to for failing to be identified as "prior art"; and claims 1-4 were rejected under 35 USC 102(b) as being anticipated by U.S. patent No. 5,689,144 to Williams.

In response to the objection to figure 1, Applicants have submitted herewith a replacement sheet including Figure 1 identified as "Prior Art." No further objection is therefore anticipated.

Regarding the Williams patent, the double gate FET disclosed therein is a so-called ordinary bulk MOSFET in which the first gate G is an insulation gate, and the second gate B is not insulated from the channel, source or drain. This can be discerned because the gate B and the source S or drain, for example, are connected to each other with a PN diode. Since a signal for biasing the PN diode in the forward direction is fed to the second gate when applying a signal to the second gate that turns the MOSFET on, a direct current 1B (shown in Figs. 12A to 12C and 16A to 16C, etc.) continues flowing even in a steady state. This continuous current flow might not have a serious adverse effect on a power MOSFET; however, the current flow may seriously adversely affect an IC because power consumption

becomes larger and larger due to current leakage. Furthermore, since the first gate G is connected to the source through the PN junction with the resistor R1 (Fig. 16A) etc., the direct current (DC) input impedance of the first gate becomes extremely small in comparison with that of the insulation gate in a transistor. Consequently, a large load is formed on the circuit that drives the MOSFET resulting in reduction of the operation speed. The maximum value of the voltage applicable to the second gate B is restricted by the PN junction.

On the other hand, the double gate FET according to the present invention has two gate electrodes which are both insulated. Since there is no DC component passing through the second gate, there is no increase in power consumption. Further, since there is no DC passing from the first gate to the second gate and to the source to thereby maintain the DC input impedance of the first gate at a high level, a load onto the gate-driving circuit is small.

In Williams, a channel is formed only on the surface of a semiconductor of a single insulation gate G face (G of Ml in Fig. 16A, for example), whereas in the present invention channels are formed on the semiconductor surfaces of the two gates faces, respectively. Moreover, unlike in Williams, the channel formation in the present invention is attained because a voltage having the same value as the voltage applied to the first gate can be applied to the second gate without any restriction imposed on the maximum value of the voltage applicable to the second gate because the two gates are insulation gates. Consequently, even in the same device area, approximately a double channel current can be utilized to sustain the characteristic feature of the double gate FET.

Further, in the present invention, the amplitude of a signal fed to the second gate is the same as that of a signal fed to the first gate, provided that, as shown in Figures 2(a) to 2(c), the second signal has a signal level shifted, a slower or faster rise time or fall time, or a slower or faster signal-applying timing as compared with the first signal. In light of these provisions, the threshold voltage during the signal-level temporal change is controlled, and

potentials of the same level are applied to the two gates in a steady state, thereby enabling the two channels to be turned on to increase the ON-current or the two channels to be turned off to reduce the leak current.

For the foregoing reasons, Williams is not believed to anticipate or render obvious the subject matter defined by claims 1-4.

Consequently, no further issues are believed to be outstanding, and the application is believed to be in condition for allowance. An early and favorable action is respectfully requested.

Respectfully submitted,

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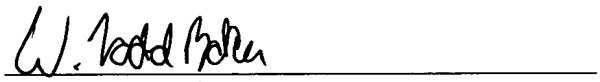

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IN THE DRAWINGS

The attached sheet of drawings includes changes to Fig. 1. This sheet, which includes Fig. 1, replaces the original sheet including Fig. 1.

Attachment: Replacement Sheet